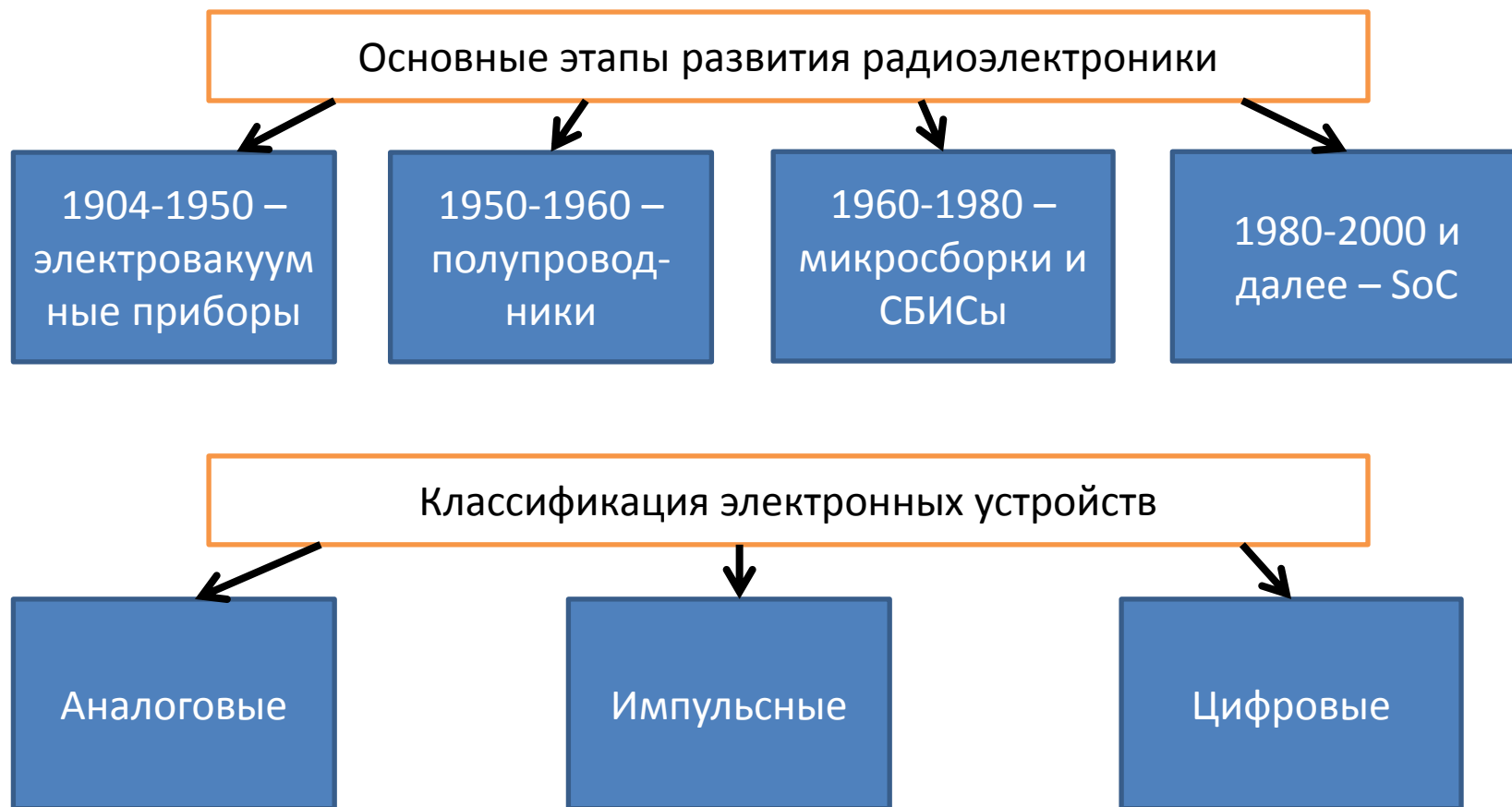
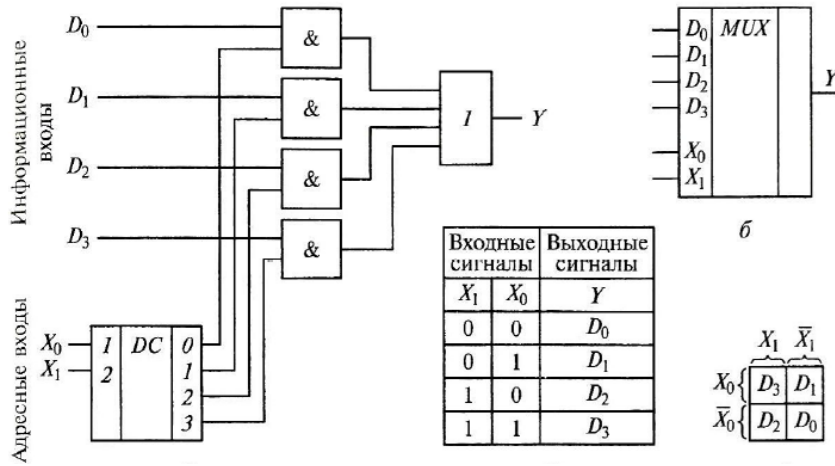


**Универсальные
программируемые интегральные
схемы в автоматизированных
системах управления
производством**

РАЗДЕЛ 1 «ВВЕДЕНИЕ В ПРОГРАММИРУЕМЫЕ ИНТЕГРАЛЬНЫЕ СХЕМЫ»

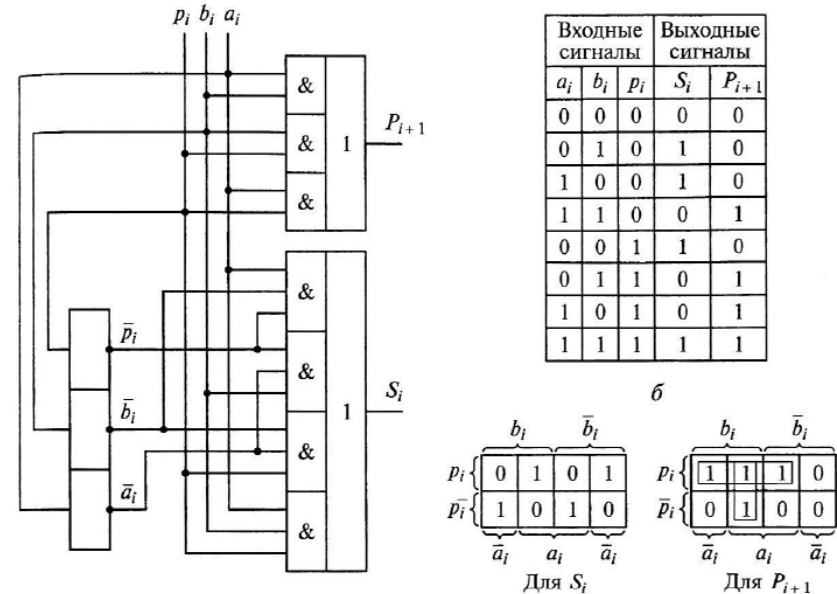


Комбинационные цифровые устройства



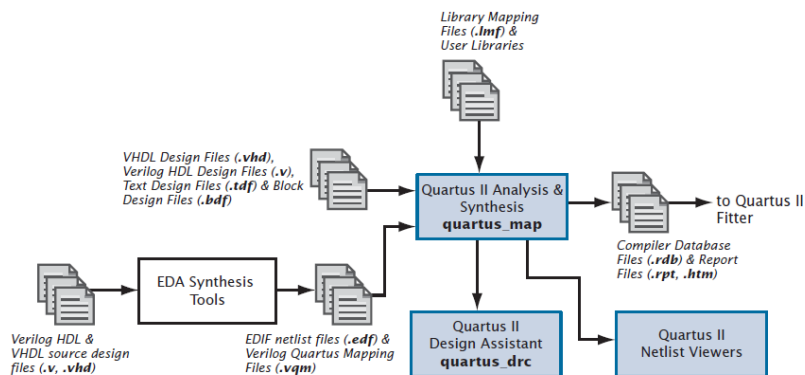
Мультиплексор

Одноразрядный сумматор



Создание проекта в Quartus II

Этап размещения и трассировки проекта в Quartus II



Окно задания целевого кристалла ПЛИС

New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family:
Family: Cyclone II
Devices: All

Show in 'Available device' list:
Package: FBGA
Pin count: 896
Speed grade: Any
 Show advanced devices
 HardCopy compatible only

Target device:
 Auto device selected by the Fitter
 Specific device selected in 'Available devices' list

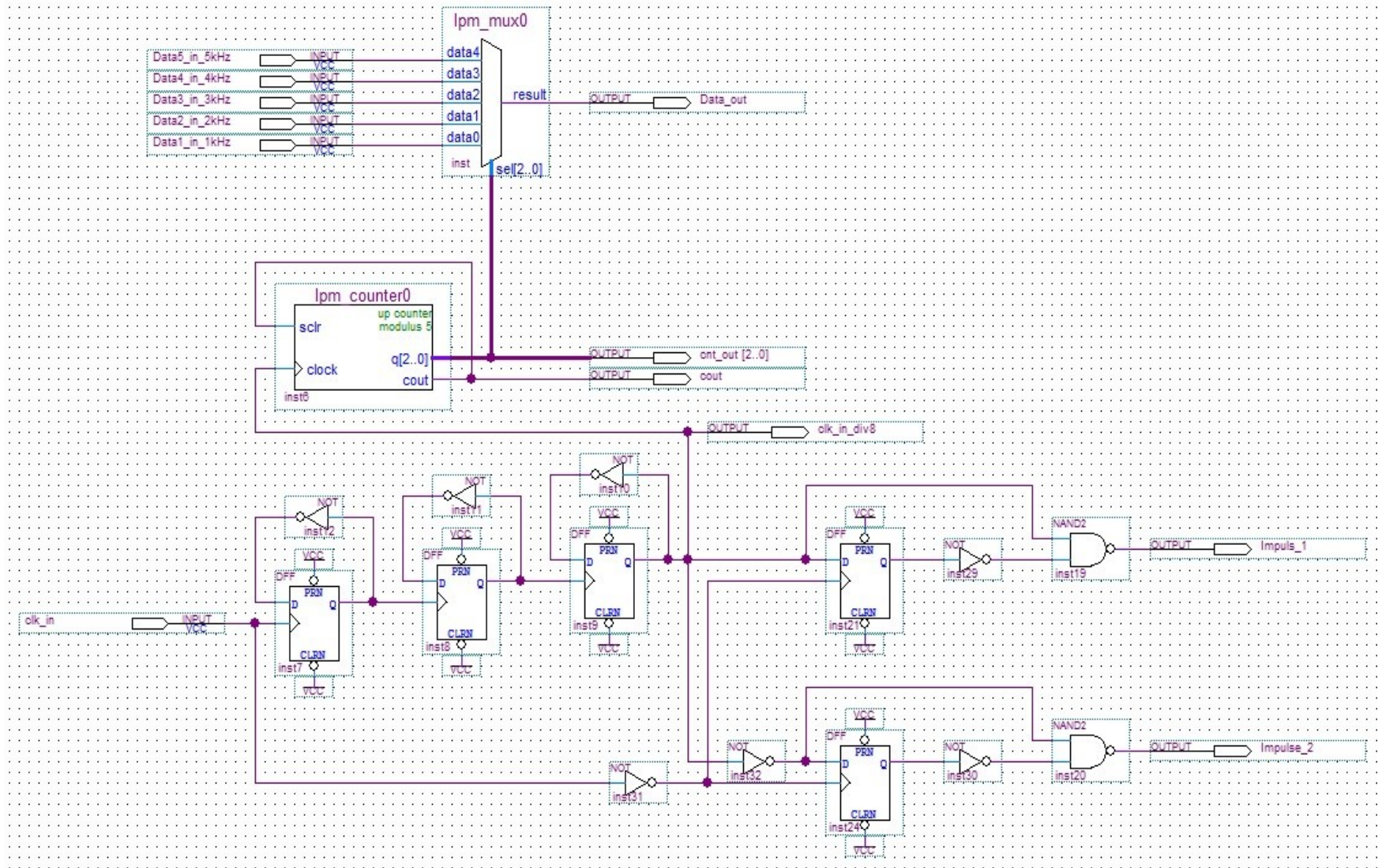
Available devices:

Name	Core v...	LEs	User I/...	Memor...	Embed...	PLL
EP2C70F896C6	1.2V	68416	622	1152000	300	4
EP2C70F896C7	1.2V	68416	622	1152000	300	4
EP2C70F896C8	1.2V	68416	622	1152000	300	4
EP2C70F896I8	1.2V	68416	622	1152000	300	4

Companion device:
HardCopy:
 Limit DSP & RAM to HardCopy device resource

< Back Next > Finish Отмена

Графическое программирование в Quartus II



Исследование проекта в Quartus II

The screenshot displays the Quartus II software interface for a project named PRJ1_MUX. The main window shows a timing diagram for the PRJ1_MUX.vwf file. The diagram is set to a Master Time Bar of 9.25 ns. The signal list includes:

Name	Value at 9.25 ns
clk_in	U 0
clk_in_div8	U X
cnt_out	U X
cout	U X
Data1_in_1kHz	U 0
Data2_in_2kHz	U 0
Data3_in_3kHz	U 0
Data4_in_4kHz	U 0
Data5_in_5kHz	U 0
Data_out	U X
Impulse_1	U X
Impulse_2	U X

The timing diagram shows the signals over time, with a pointer at 17.24 ms and an interval of 17.24 ms. The signals are plotted against a time axis from 4.375 ms to 18.125 ms.

The Project Navigator on the left shows the project structure, including the Entity PRJ1_MUX, Logic Cells (14), and LC (7). The Tasks window at the bottom left shows the compilation process, including tasks like Compile Design, Analysis & Synthesis, Analysis & Elaboration, Fitter (Place & Route), Assembler, and Classic Timing Analysis.